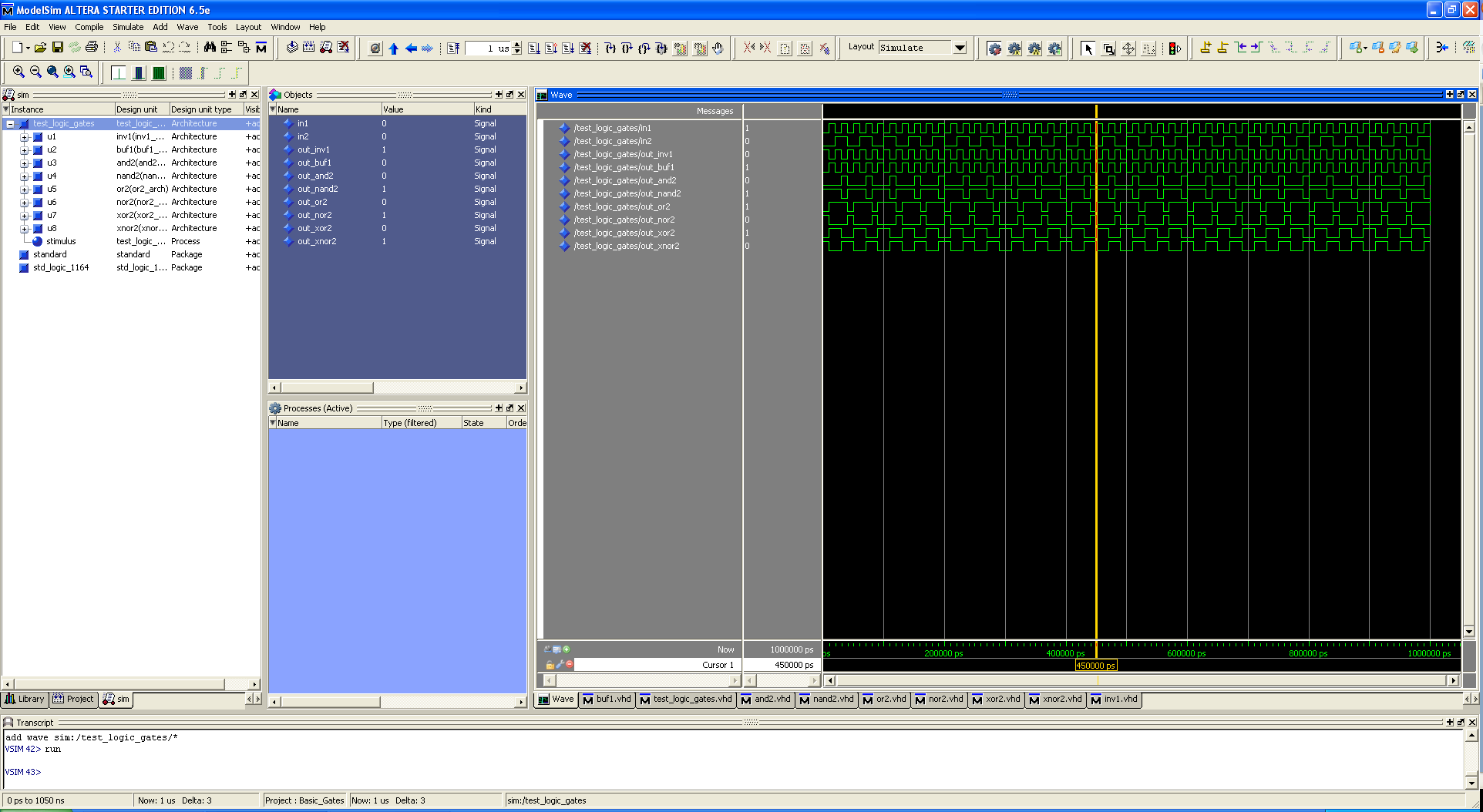
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Lameres/EE 367

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Homework #2: Simulating Basic Gates in Modelsim

**Basic Gates Waveforms**



**VHDL Code**

Buf1.vhd

library IEEE; -- this library adds additional capability for VHDL use IEEE.STD\_LOGIC\_1164.ALL; -- this package has "STD\_LOGIC" data types

entity buf1 is

port (In1 : in STD\_LOGIC;

Out1 : out STD\_LOGIC);

end entity buf1;

architecture buf1\_arch of buf1 is

begin

Out1 <= In1;

end architecture buf1\_arch;

and2.vhd

library IEEE; -- this library adds additional capability for VHDL

use IEEE.STD\_LOGIC\_1164.ALL; -- this package has "STD\_LOGIC" data types

entity and2 is

port (In1, In2 : in STD\_LOGIC;

Out1 : out STD\_LOGIC);

end entity and2;

architecture and2\_arch of and2 is

begin

Out1 <= In1 and In2;

end architecture and2\_arch;

nand2.vhd

library IEEE; -- this library adds additional capability for VHDL

use IEEE.STD\_LOGIC\_1164.ALL; -- this package has "STD\_LOGIC" data types

entity nand2 is

port (In1, In2 : in STD\_LOGIC;

Out1 : out STD\_LOGIC);

end entity nand2;

architecture nand2\_arch of nand2 is

begin

Out1 <= In1 nand In2;

end architecture nand2\_arch;

or2.vhd

library IEEE; -- this library adds additional capability for VHDL

use IEEE.STD\_LOGIC\_1164.ALL; -- this package has "STD\_LOGIC" data types

entity or2 is

port (In1, In2 : in STD\_LOGIC;

Out1 : out STD\_LOGIC);

end entity or2;

architecture or2\_arch of or2 is

begin

Out1 <= In1 or In2;

end architecture or2\_arch;

nor2.vhd

library IEEE; -- this library adds additional capability for VHDL

use IEEE.STD\_LOGIC\_1164.ALL; -- this package has "STD\_LOGIC" data types

entity nor2 is

port (In1, In2 : in STD\_LOGIC;

Out1 : out STD\_LOGIC);

end entity nor2;

architecture nor2\_arch of nor2 is

begin

Out1 <= In1 nor In2;

end architecture nor2\_arch;

xor2.vhd

library IEEE; -- this library adds additional capability for VHDL

use IEEE.STD\_LOGIC\_1164.ALL; -- this package has "STD\_LOGIC" data types

entity xor2 is

port (In1, In2 : in STD\_LOGIC;

Out1 : out STD\_LOGIC);

end entity xor2;

architecture xor2\_arch of xor2 is

begin

Out1 <= In1 xor In2;

end architecture xor2\_arch;

xnor2.vhd

library IEEE; -- this library adds additional capability for VHDL

use IEEE.STD\_LOGIC\_1164.ALL; -- this package has "STD\_LOGIC" data types

entity xnor2 is

port (In1, In2 : in STD\_LOGIC;

Out1 : out STD\_LOGIC);

end entity xnor2;

architecture xnor2\_arch of xnor2 is

begin

Out1 <= In1 xnor In2;

end architecture xnor2\_arch;